IR-2053 DIV (2-2500)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of:

Thomas Herman

Serial No.: 09/723,655

Filed: November 28, 2000

Date: February 9, 2004

Group Art Unit: 2815

For: PROCESS FOR MANUFACTURING A LOW VOLTAGE MOSFET POWER DEVICE HAVING A MINIMUM FIGURE OF MERIT

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Sir:

This appeal is taken from the Examiner's final rejection dated July 9, 2003, in connection with the above-identified application. The Notice of Appeal was filed in the United States Patent and Trademark Office on December 8, 2003.

I. Status of Claims

Claims 9-14, 21 and 22 stand rejected and are pending on appeal.

II. Real Party in Interest

The real party in interest is the assignee, International Rectifier Corporation.

III. Related Appeals and Interferences

The applicants, the assignee and the undersigned attorneys are not aware of any related appeals or interferences.

IV. Status of Amendments

An Amendment/Submission containing arguments regarding the patentability of the claims was filed after the final rejection on October 8, 2003, and was considered.

V. Summary of Invention

The present invention is directed at a method for processing a power semiconductor device. According to the invention, polysilicon stripes 61, which are intended to be used as gate electrodes, define a mask for the formation of three sequential regions, the first being a base 80 (or channel) diffusion, the second being a source diffusion 81 and the third being a higher concentration (high conductivity/low resistivity) base region 85 which underlies the first base and which does not invade the invertible channel (region of base 80 below gate electrode) formed by the first base and source. After implanting the third region, a short thermal step is carried out to activate the dopants. Thereafter, sidewall spacers 96 are formed on the sidewalls of the polysilicon stripes 61.

As a result of the present invention, the low resistivity base region 85 (third region) is formed to extend as far as possible laterally under the source region 81 (second region) without application of a long thermal step. By avoiding a long thermal step, the lateral expansion of the

body region 80 can be avoided. As a result, the invertible channel region can be kept short. It is well known that shorter channels lead to lower On resistance (Rdson).

Furthermore, the lateral extent of the low resistivity region 85 under source region 81 is increased, thereby reducing the resistance under source region 81. As a result, the ruggedness of the device can be improved.

In addition, as a result of a process according to the present invention, the thickness of the spacers is no longer of critical interest in that the spacers are not used to control the size of other features in the device. By eliminating a critical feature, processing is simplified. That is, simply stated, by removing a complexity (critical dimension of the spacers) from the process fewer problems can occur during the processing, thereby increasing yield. An increase in yield improves cost-effectiveness which is of great industrial importance in the competitive field of power semiconductor processing.

Thus, claim 9 calls for:

9. The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a

mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes into said silicon surface using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions.

VI. Issues on Appeal

Whether claims 9-14, 21 and 22 are obvious under 35 U.S.C. 103 (a) in view of the art of record.

VII. Grouping of Claims

Claims 9-14, 21 and 22 stand or fall together.

VIII. Argument

In an office action dated March 6, 2003, claim 9 was rejected under 35 U.S.C. §103(a) over Davies, U.S. Patent No. 5,155,052 in view of Ajit et al., U.S. Patent No. 5,474,946. It was set forth that Davies teaches, among other limitations of claim 9, using the stripes of oxide and polysilicon for forming the second base diffusions as set forth in claim 9.

It is respectfully submitted that Davies does not teach using the oxide and polysilicon stripes in forming the second base diffusions. Indeed, Davies teaches the opposite.

Davies teaches forming sidewall spacers 18 before forming low resistivity regions 17. That is, sidewall spacers 18 are used for positioning low resistivity regions. Col. 4, line 12-14. As a result, contrary to the results achieved by the present invention, the low resistivity regions 17 do not extend laterally as far as possible. Thus, the resistance under the source regions is not reduced as far as possible, which means that the ruggedness of the device is not as good as a device produced by a process according to the present invention.

In addition, Davies teaches that using the sidewall spacers 18 is critical in manufacturing his device:

> Width of sidewall spacer 18 is a critical feature of the present invention, and is determined by thickness of the deposited layer from which sidewall spacer 18 was etched. In a preferred embodiment, spacer 18 is about as wide as thickness of polysilicon gate 14, or about 0.3-0.8 microns. Thinner spacer width corresponds to smaller source depth for optimal performance, thus actual thickness is a design choice based on diffusion and film deposition technology. Width of sidewall spacer 18 determines relative spacing between source 15, base 12, and low resistivity region 17. If this spacing is too small, or varies widely due to the process control of forming spacer 18, low resistivity region 17 will extend into channel 26, destroying the device. For example, it has been found that if a thin oxide, analogous to oxide 15 shown in

> FIG. 1, is used rather than a sidewall spacer 18, insufficient separation between base 12 and low resistivity region 17 is provided, and correspondingly low yields result.
>
> Col. 4, lines 25-43.

The excerpt noted above indicates that Davies actually teaches away from using the oxide and polysilicon stripes as a mask in forming the second base regions (low resistivity regions 17). It is respectfully submitted, therefore, that Davies does not teach or suggest using the oxide and polysilicon stripes as a mask for forming the second based diffusions.

In an office action dated July 9, 2003, the Examiner responded that Davies at Col. 4, lines 38-43 teaches a "situation where sidewall spacers are not used in implanting the low resistivity regions 17." Col. 4, lines 38-43 provide:

> For example, it has been found that if a thin oxide, analogous to oxide 15 shown in FIG. 1, is used rather than a sidewall spacer 18, insufficient separation between base 12 and low resistivity region 17 is provided, and correspondingly low yields result.

It is quite clear that in the example provided by Davies a thin oxide wall (i.e. a thin sidewall) is used in preparing the device. That is, the example, contrary to the position taken in the Office Action, does not call for a "situation where sidewall spacers are not used".

Furthermore, Davies also states that if the spacing provided by the sidewall spacers is "too small, or varies widely due to the process control of forming spacer 18, low resistivity region 17 will extend into channel 26, destroying the device."

Thus, Davies quite clearly says that too thin a sidewall destroys the device. From this statement it is logical to conclude that eliminating the sidewalls destroys the device.

It follows, as previously argued, that Davies teaches away from the invention.

In response, it has been stated that Davies teaches that eliminating the sidewall spacers only results in low yields, which, according to the Office Action, does not mean that the process taught by Davies produces an inoperative device.

As noted above, Davies does not in fact provide an example in which no sidewall is used. The example provided uses a thin sidewall.

In addition, it is quite clear from the portion cited that Davies considers the sidewalls of critical importance to practicing his process.

Moreover, low yield as used by Davies, and in the context of semiconductor processing, teaches those skilled in the art that if the sidewalls are too thin the process will fail to regularly produce operative devices. It is respectfully suggested that "low yield" in Davies is intended to discourage those skilled in the art from omitting the sidewalls, rather than give them hope that some operative devices, however low in number, may be obtained by omitting the sidewalls. Thus, the term low yield teaches away from the invention.

It is respectfully submitted that the art of record neither anticipates the subject matter of claim 9, nor does it make claim 9 obvious. The rejection should be reversed.

Claims 10-14, 21 and 22 depend from claim 9 and thus include its limitations. Each of these claims includes other limitations which in combination with those of claim 9 are not shown or suggested by the art of record.

IX. Conclusion

Claims 9-14, 21 and 22 are allowable over the art of record.

Our check No. 14203, which includes the amount of $330 to cover the appeal brief is attached hereto. This brief is being submitted in triplicate in accordance with 37 C.F.R. 1.192 and applicant reserves the right to request an oral hearing upon receipt of the Examiner's Answer.

If this communication is being filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing the required papers by the number of months which will avoid abandonment under 37 C.F.R §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 9, 2004

Kourosh Salehi
Name of applicant, assignee or Registered Representative

Signature

February 9, 2004
Date of Signature

KS:gl

Respectfully submitted,

Kourosh Salehi
Registration No.: 43,898
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

APPENDIX OF CLAIMS ON APPEAL

9. The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes into said silicon surface using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions.

10. The process of claim 9, wherein said polysilicon stripes have a width of 3.1 microns and a spacing of 1.25 microns.

11. The process of claim 9 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

12. The process of claim 10 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

13. The process of claim 9 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. The process of claim 12 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

21. The process of claim 9 wherein said polysilicon stripes are spaced 1.5 microns apart.

22. The process of claim 9 wherein said polysilicon stripes are spaced 3.2 to 3.4 microns wide.

IR-2053 DIV (2-2500)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of:

Thomas Herman

Date: February 9, 2004

Serial No.: 09/723,655

Group Art Unit: 2815

Filed: November 28, 2000

For: PROCESS FOR MANUFACTURING A LOW VOLTAGE MOSFET POWER DEVICE HAVING A MINIMUM FIGURE OF MERIT

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Sir:

This appeal is taken from the Examiner's final rejection dated July 9, 2003, in connection with the above-identified application. The Notice of Appeal was filed in the United States Patent and Trademark Office on December 8, 2003.

I. Status of Claims

Claims 9-14, 21 and 22 stand rejected and are pending on appeal.

II. Real Party in Interest

The real party in interest is the assignee, International Rectifier Corporation.

III. Related Appeals and Interferences

The applicants, the assignee and the undersigned attorneys are not aware of any related appeals or interferences.

IV. Status of Amendments

An Amendment/Submission containing arguments regarding the patentability of the claims was filed after the final rejection on October 8, 2003, and was considered.

V. Summary of Invention

The present invention is directed at a method for processing a power semiconductor device. According to the invention, polysilicon stripes 61, which are intended to be used as gate electrodes, define a mask for the formation of three sequential regions, the first being a base 80 (or channel) diffusion, the second being a source diffusion 81 and the third being a higher concentration (high conductivity/low resistivity) base region 85 which underlies the first base and which does not invade the invertible channel (region of base 80 below gate electrode) formed by the first base and source. After implanting the third region, a short thermal step is carried out to activate the dopants. Thereafter, sidewall spacers 96 are formed on the sidewalls of the polysilicon stripes 61.

As a result of the present invention, the low resistivity base region 85 (third region) is formed to extend as far as possible laterally under the source region 81 (second region) without application of a long thermal step. By avoiding a long thermal step, the lateral expansion of the

body region 80 can be avoided. As a result, the invertible channel region can be kept short. It is well known that shorter channels lead to lower On resistance (Rdson).

Furthermore, the lateral extent of the low resistivity region 85 under source region 81 is increased, thereby reducing the resistance under source region 81. As a result, the ruggedness of the device can be improved.

In addition, as a result of a process according to the present invention, the thickness of the spacers is no longer of critical interest in that the spacers are not used to control the size of other features in the device. By eliminating a critical feature, processing is simplified. That is, simply stated, by removing a complexity (critical dimension of the spacers) from the process fewer problems can occur during the processing, thereby increasing yield. An increase in yield improves cost-effectiveness which is of great industrial importance in the competitive field of power semiconductor processing.

Thus, claim 9 calls for:

9. The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a

mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes into said silicon surface using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions.

VI. Issues on Appeal

Whether claims 9-14, 21 and 22 are obvious under 35 U.S.C. 103 (a) in view of the art of record.

VII. Grouping of Claims

Claims 9-14, 21 and 22 stand or fall together.

VIII. Argument

In an office action dated March 6, 2003, claim 9 was rejected under 35 U.S.C. §103(a) over Davies, U.S. Patent No. 5,155,052 in view of Ajit et al., U.S. Patent No. 5,474,946. It was set forth that Davies teaches, among other limitations of claim 9, using the stripes of oxide and polysilicon for forming the second base diffusions as set forth in claim 9.

It is respectfully submitted that Davies does not teach using the oxide and polysilicon stripes in forming the second base diffusions. Indeed, Davies teaches the opposite.

Davies teaches forming sidewall spacers 18 before forming low resistivity regions 17. That is, sidewall spacers 18 are used for positioning low resistivity regions. Col. 4, line 12-14. As a result, contrary to the results achieved by the present invention, the low resistivity regions 17 do not extend laterally as far as possible. Thus, the resistance under the source regions is not reduced as far as possible, which means that the ruggedness of the device is not as good as a device produced by a process according to the present invention.

In addition, Davies teaches that using the sidewall spacers 18 is critical in manufacturing his device:

> Width of sidewall spacer 18 is a critical feature of the present invention, and is determined by thickness of the deposited layer from which sidewall spacer 18 was etched. In a preferred embodiment, spacer 18 is about as wide as thickness of polysilicon gate 14, or about 0.3-0.8 microns. Thinner spacer width corresponds to smaller source depth for optimal performance, thus actual thickness is a design choice based on diffusion and film deposition technology. Width of sidewall spacer 18 determines relative spacing between source 15, base 12, and low resistivity region 17. If this spacing is too small, or varies widely due to the process control of forming spacer 18, low resistivity region 17 will extend into channel 26, destroying the device. For example, it has been found that if a thin oxide, analogous to oxide 15 shown in

> FIG. 1, is used rather than a sidewall spacer 18, insufficient separation between base 12 and low resistivity region 17 is provided, and correspondingly low yields result.
>
> Col. 4, lines 25-43.

The excerpt noted above indicates that Davies actually teaches away from using the oxide and polysilicon stripes as a mask in forming the second base regions (low resistivity regions 17). It is respectfully submitted, therefore, that Davies does not teach or suggest using the oxide and polysilicon stripes as a mask for forming the second based diffusions.

In an office action dated July 9, 2003, the Examiner responded that Davies at Col. 4, lines 38-43 teaches a "situation where sidewall spacers are not used in implanting the low resistivity regions 17." Col. 4, lines 38-43 provide:

> For example, it has been found that if a thin oxide, analogous to oxide 15 shown in FIG. 1, is used rather than a sidewall spacer 18, insufficient separation between base 12 and low resistivity region 17 is provided, and correspondingly low yields result.

It is quite clear that in the example provided by Davies a thin oxide wall (i.e. a thin sidewall) is used in preparing the device. That is, the example, contrary to the position taken in the Office Action, does not call for a "situation where sidewall spacers are not used".

Furthermore, Davies also states that if the spacing provided by the sidewall spacers is "too small, or varies widely due to the process control of forming spacer 18, low resistivity region 17 will extend into channel 26, destroying the device."

Thus, Davies quite clearly says that too thin a sidewall destroys the device. From this statement it is logical to conclude that eliminating the sidewalls destroys the device.

It follows, as previously argued, that Davies teaches away from the invention.

In response, it has been stated that Davies teaches that eliminating the sidewall spacers only results in low yields, which, according to the Office Action, does not mean that the process taught by Davies produces an inoperative device.

As noted above, Davies does not in fact provide an example in which no sidewall is used. The example provided uses a thin sidewall.

In addition, it is quite clear from the portion cited that Davies considers the sidewalls of critical importance to practicing his process.

Moreover, low yield as used by Davies, and in the context of semiconductor processing, teaches those skilled in the art that if the sidewalls are too thin the process will fail to regularly produce operative devices. It is respectfully suggested that "low yield" in Davies is intended to discourage those skilled in the art from omitting the sidewalls, rather than give them hope that some operative devices, however low in number, may be obtained by omitting the sidewalls. Thus, the term low yield teaches away from the invention.

It is respectfully submitted that the art of record neither anticipates the subject matter of claim 9, nor does it make claim 9 obvious. The rejection should be reversed.

Claims 10-14, 21 and 22 depend from claim 9 and thus include its limitations. Each of these claims includes other limitations which in combination with those of claim 9 are not shown or suggested by the art of record.

IX. Conclusion

Claims 9-14, 21 and 22 are allowable over the art of record.

Our check No. 14203, which includes the amount of $330 to cover the appeal brief is attached hereto. This brief is being submitted in triplicate in accordance with 37 C.F.R. 1.192 and applicant reserves the right to request an oral hearing upon receipt of the Examiner's Answer.

If this communication is being filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing the required papers by the number of months which will avoid abandonment under 37 C.F.R §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 9, 2004

Kourosh Salehi
Name of applicant, assignee or Registered Representative

Signature

February 9, 2004
Date of Signature

KS:gl

Respectfully submitted,

Kourosh Salehi
Registration No.: 43,898
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

APPENDIX OF CLAIMS ON APPEAL

9. The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes into said silicon surface using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions.

10. The process of claim 9, wherein said polysilicon stripes have a width of 3.1 microns and a spacing of 1.25 microns.

11. The process of claim 9 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

12. The process of claim 10 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

13. The process of claim 9 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. The process of claim 12 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

21. The process of claim 9 wherein said polysilicon stripes are spaced 1.5 microns apart.

22. The process of claim 9 wherein said polysilicon stripes are spaced 3.2 to 3.4 microns wide.